

FIG. 1

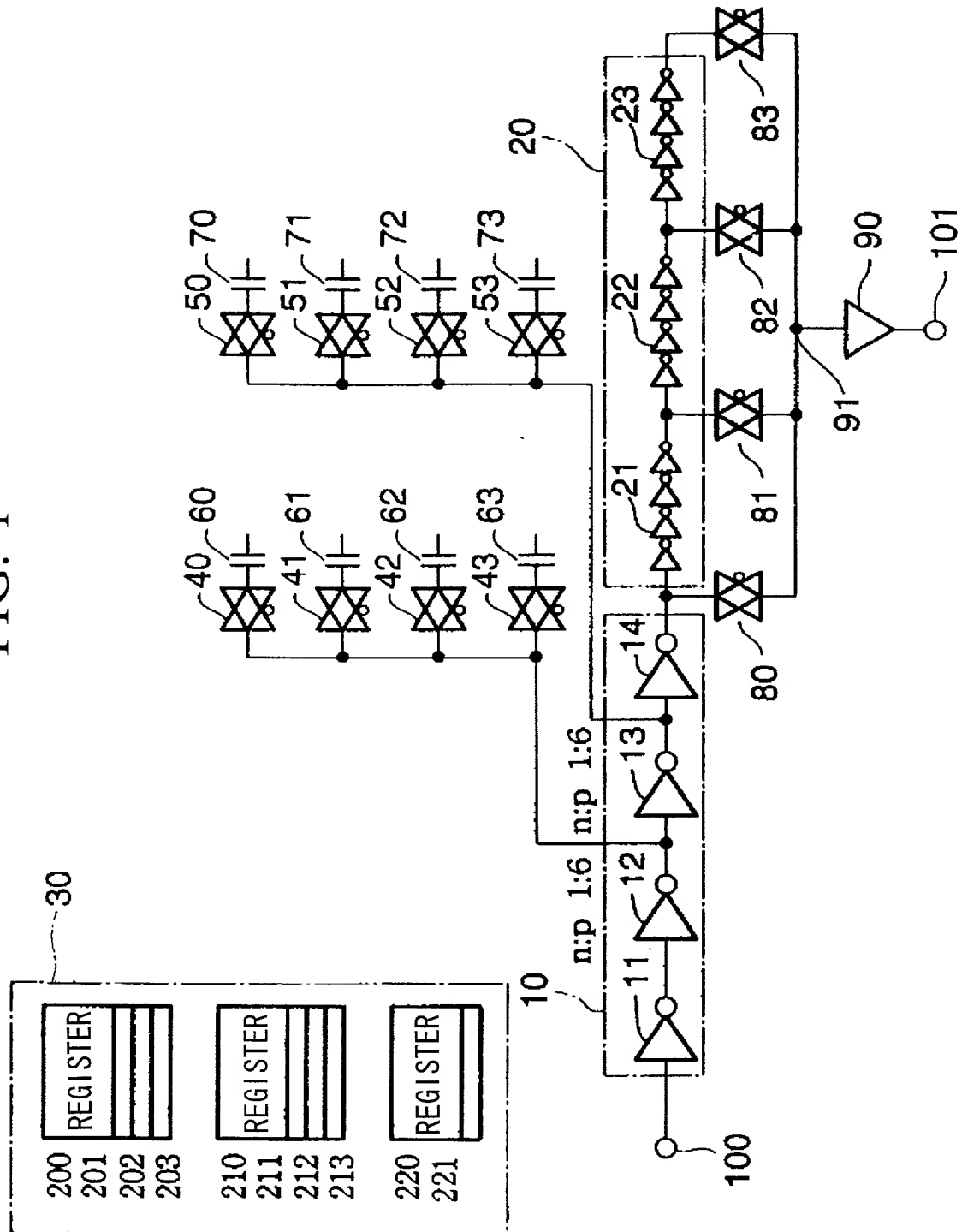


FIG. 2

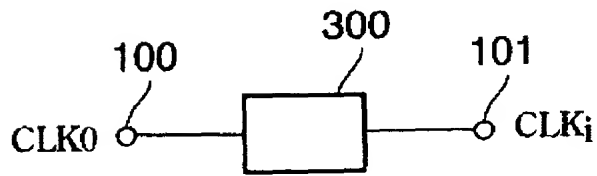


FIG. 4

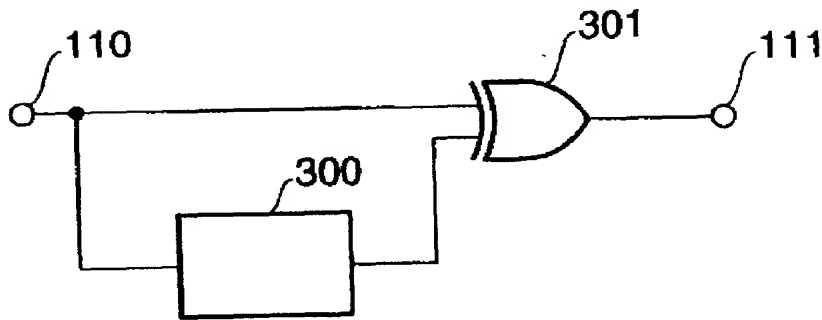


FIG. 8

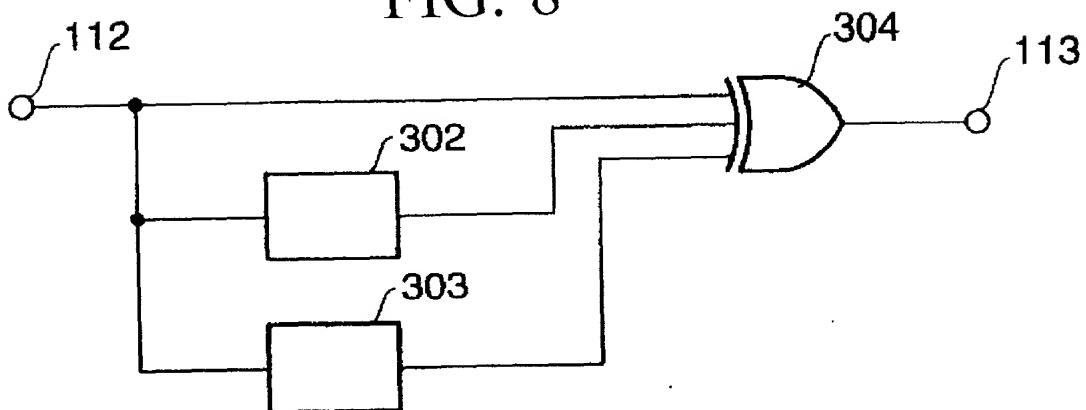


FIG. 3A

REFERENCE
CLOCK CLK0



FIG. 3B

OUTPUT SIGNAL
CLKi



FIG. 5A

REFERENCE
CLOCK
CLK0



FIG. 5B

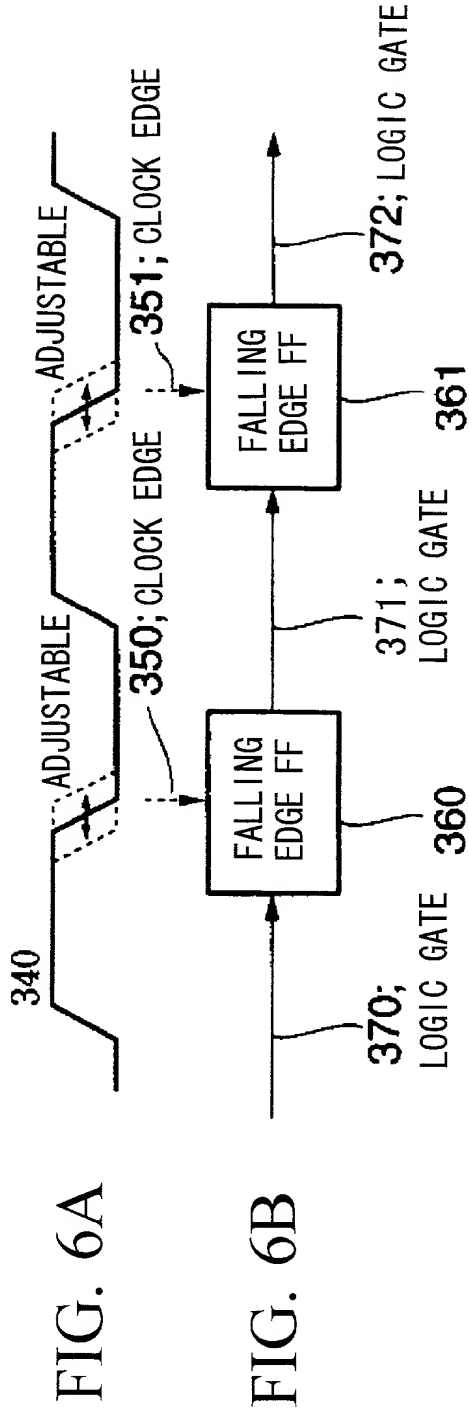
CLOCK
CLKj



FIG. 5C

OUTPUT
CLOCK
CLKn





Title: DELAY ADJUSTMENT CIRCUIT
AND A CLOCK GENERATING CIRCUIT
USING THE SAME

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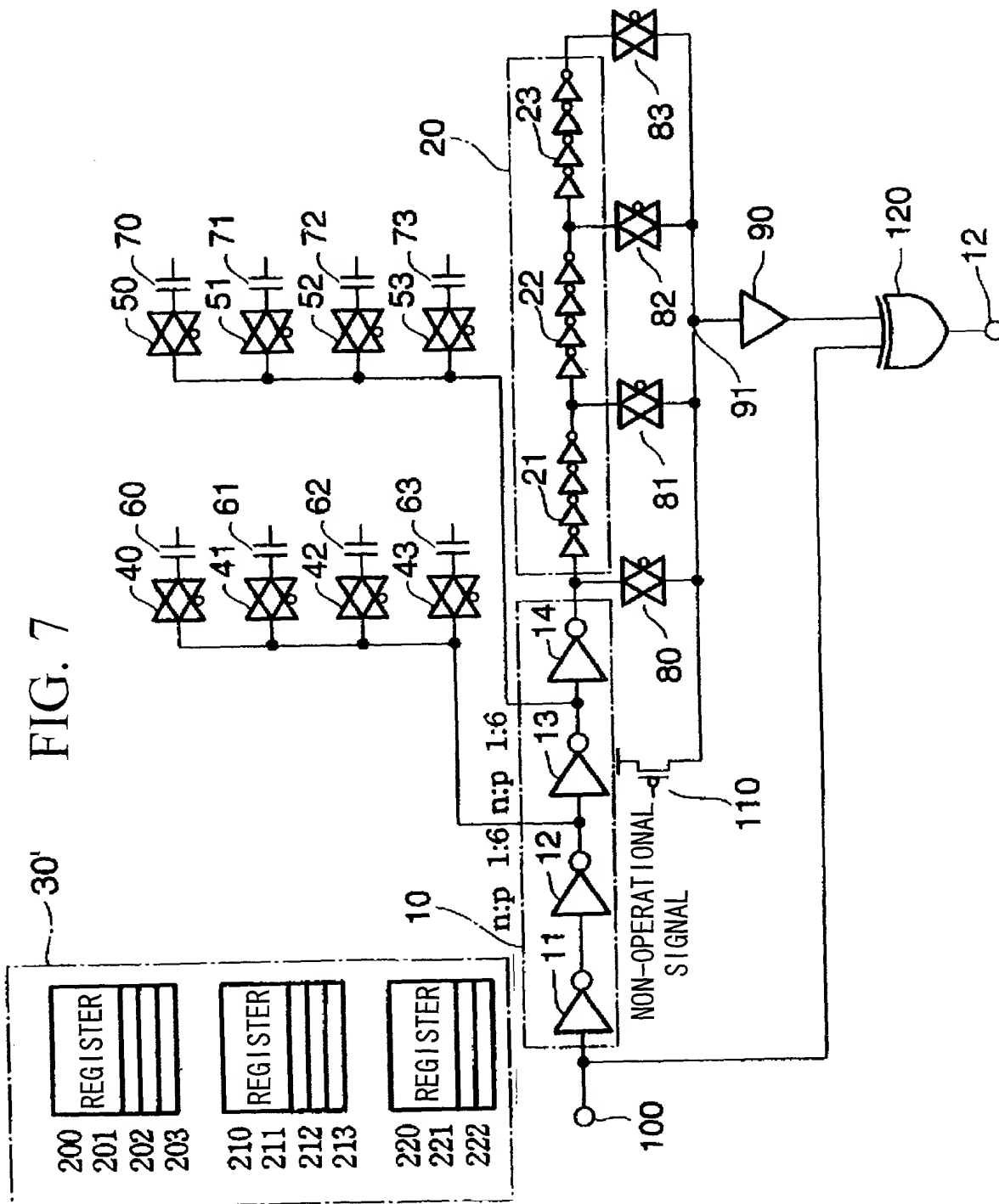
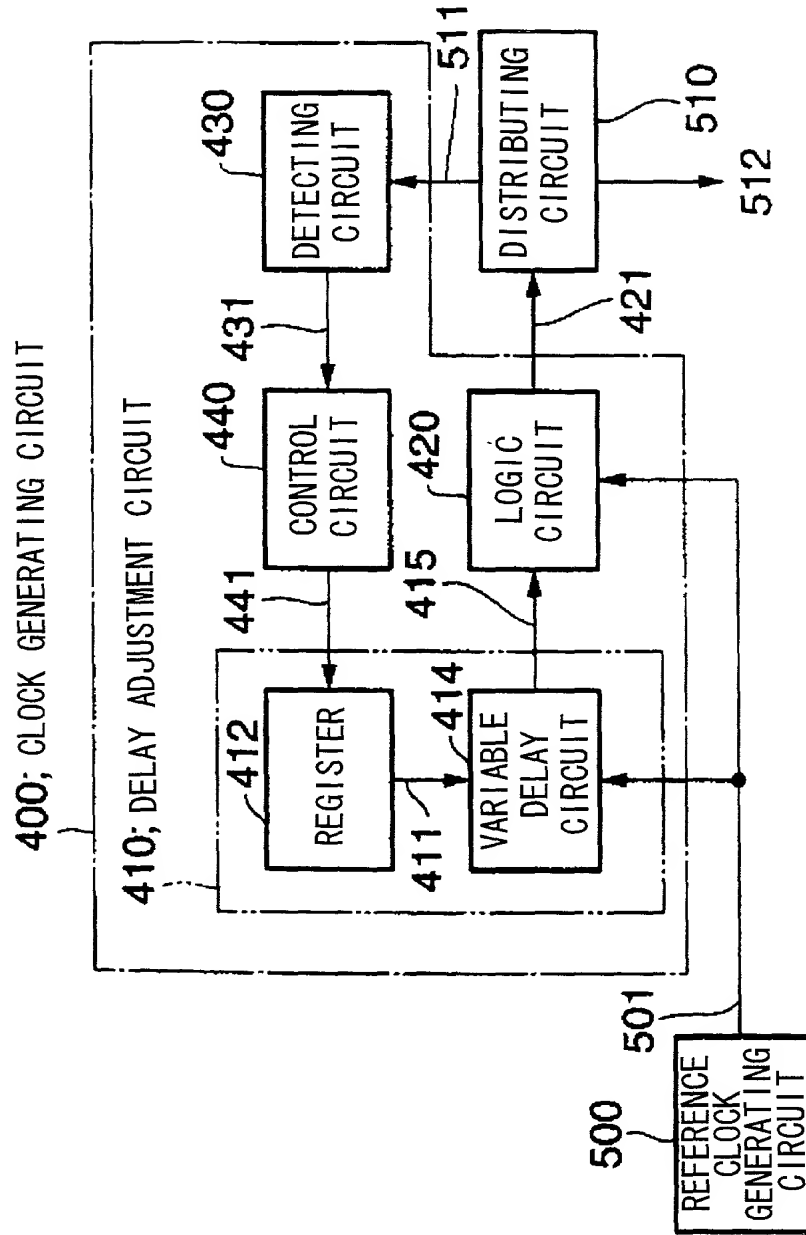


FIG. 10



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FIG. 11

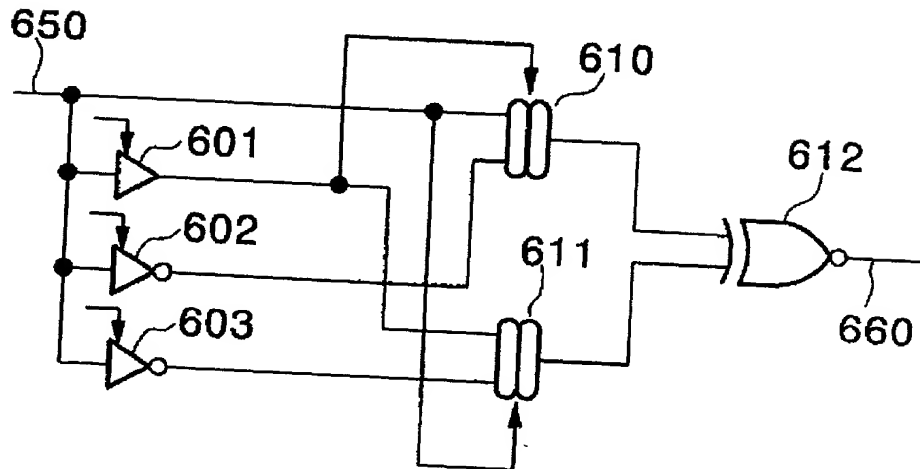
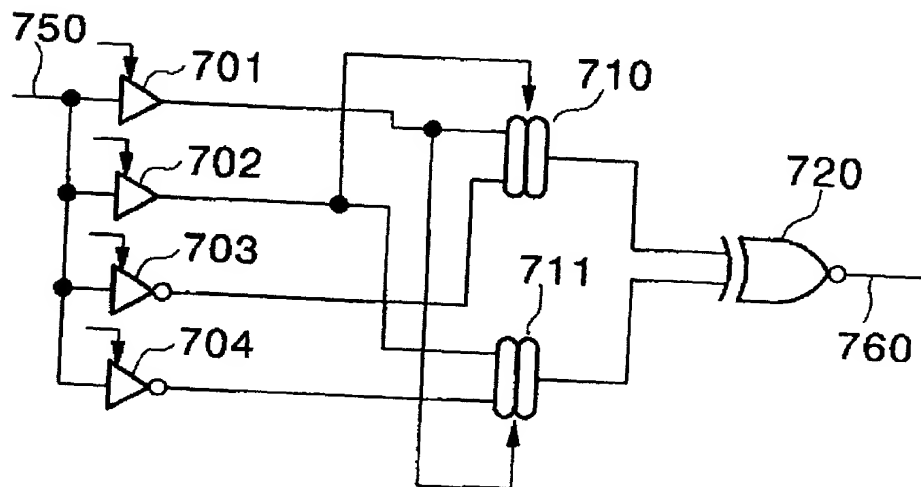
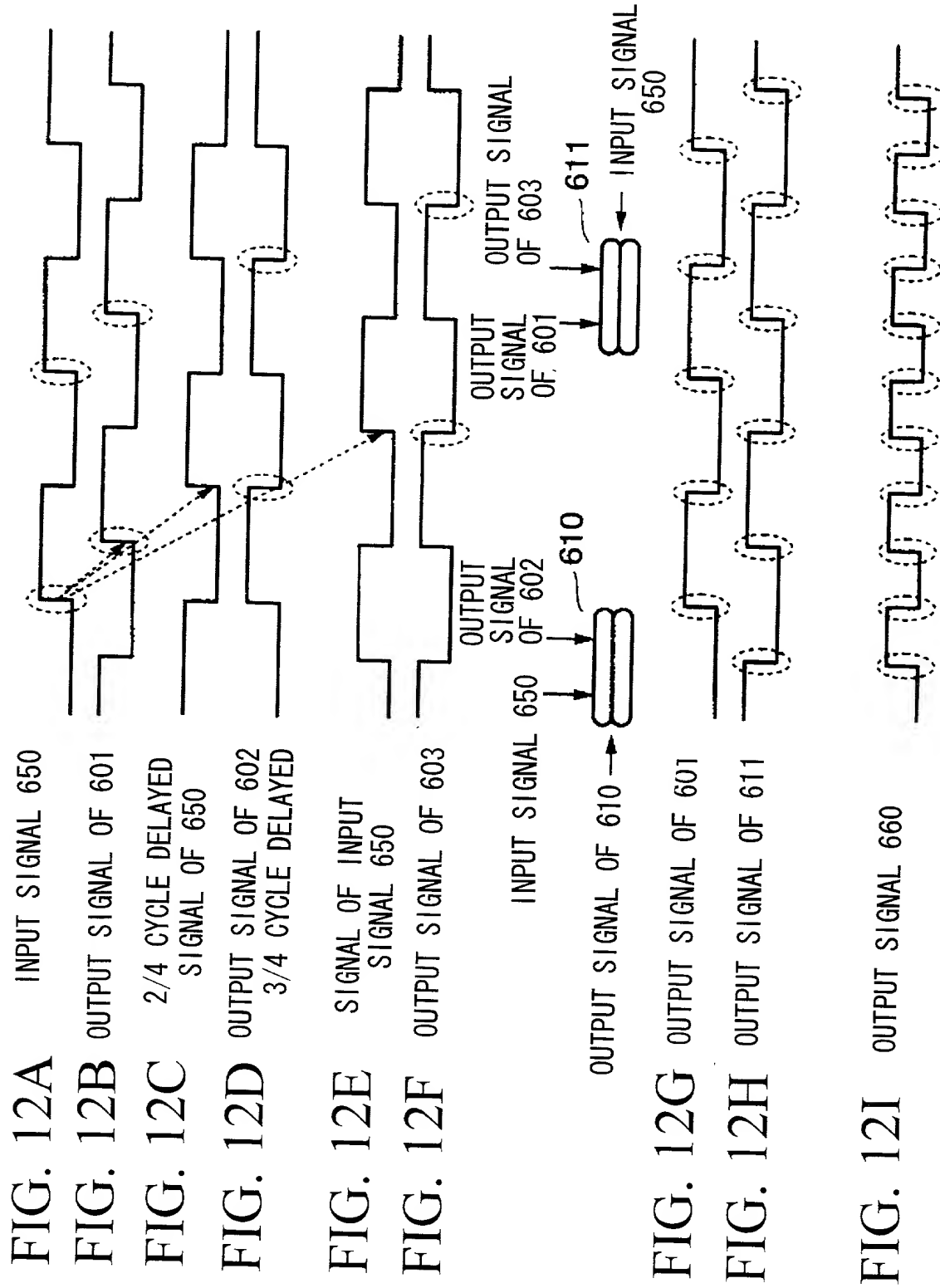


FIG. 13





Title: DELAY ADJUSTMENT CIRCUIT
AND A CLOCK GENERATING CIRCUIT
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FIG. 14

